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END TERM EXAMINATION

SECOND SEMESTER [BCA] MAY-JUNE-2013

Paper Code: BCA106 **Subject: Digital Electronics (New)**

Time : 3 Hours **Maximum Marks :75**

Note: Attempt any five questions including Q.no.1 which is compulsory. Select one question from each unit.

Q1. (a) Design a Full Adder circuit using only NANAD gates only. (5)

(b) State and explain the DeMorgen's theorem which converts a sum into a product from and vice versa. (5)

(c) What is Multiplexer? Explain the difference between MUX and DEMUX. (5)

(d) Explain Binary Multiplier. (5)

(e) Simplify the following function in Sum of product from using four variable Karnaugh's map. Draw the resulting logic diagram. (5)

$F(A,B,C,D) = \Sigma (0,1,2,4,5,7,11,15)$

Unit- I

Q.2. (a) (i) Simplify the Expression $AB + \overline{AC} + A\overline{B}C$ (AB+c) (3)

(ii) Simplify the given Boolean Expression (3)

$Y = \overline{A}\,\overline{B}\,\overline{C} + \overline{A}\,B\,\overline{C} + A\,\overline{B}\,\overline{C} + A\,B\,\overline{C}$

(b) Explain what is meant by logic family. Describe three major difference between RTL and DTL. (6.5)

Q.3. (a) Explain how the basic gates can be realized using NAND gates. Draw the useful Diagram. (6.5)

(b) Implement $Y = \overline{AB} + A + \overline{B + C}$ using NAND gates only. (6)

Unit – II

Q.4 (a) Draw a Multiplexer using only NAND gates which selects from four inputs A0 to A3 using two select inputs S0 and S1. (6.5)

(b) Implement the following function using a Multiplexer

P.T.O.

$F(A,B,C) = \Sigma(1,22,5,6)$ (6)

Q5. (a) How does an encoder differ from decoder? Design 3 X 8 decoder. (6.5)

(b) Design a 4 bit parallel binary adder. (6)

Unit- III

Q.6. (a) Explain in detail the construction and working universal / Bidirectional shift register. (6)

(b) Explain the operation of Master – slave Flip Flop and show how the race around condition is eliminated in it? (6.5)

Q7. (a) Explain the function of a D flip flop using a suitable diagram and discuss how it works as a latch? (6)

(b) How an SR flip flop can be converted into JK flip flop? Give the truth table of JK flip flop Flop. (6.5)

Unit-IV

Q8. (a) Design a MOD 7 binary counter. Draw its state diagram and circuit. (6)

(b) What is a modulus counter? Draw the logic diagram of a 4 bit binary ripple counter using flip-flops that trigger on the positive edge transition. (6.5)

Q.9. (a) What is ROM? Explain the terms volatile memory and non-volatile memory. (6)

(b) What is a ripple counter? Explain the difference the performance of asynchronous and synchronous counter. (6.5)

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END TERM EXAMINATION

SECOND SEMESTER [BCA] MAY- JUNE 2015

Paper Code: BCA-106 ***Subject: Digital Electronics (Batch 2011 onwards)***

Time: 3 Hours ***Maximum Marks: 75***

Note: Attempt any five questions including Q.No 1 which is compulsory. Select one question from each unit.

Q1 (a) State and Prove the Demorgan's theorems. **(4)**
(b) Desgin a full adder using the NAND gates only. **(4)**
(c) What is a multiplexer? Desgin a 32 to 1 multiplexer using the 8 to 1 multiplexers. **(4)**
(d) What is a D flip flop? Show how SR flip flop can be converted to D flip flop. **(4)**
(e) What is a ripple counter? Explain the difference between the performance of asynchronous and synchronous counters. **(4)**
(f) Explain the working of bi directional shift register with logic diagram. **(5)**

UNIT-I

Q2 (a) What is Gray code? Why it is important? List features of BCD and Excess-3codes. **(6)**
(b) What are Universal gate? Obtain EX-OR operation with universal gates. **(3.5)**
(c) convert the following octal numbers to hexadecimal numbers: **(3)**
(i) 137
(ii) 1275
(iii) 673

Q3 (a) Simplify the expression $Y = \sum_m (7,9,10,11,12,13,14,15)$ using the K-map method. **(6.5)**
(b) Realize $Y = A + BC\overline{D}$ using NAND gates only. **(6)**

UNIT-II

Q4 (a) Design a 4 bit parallel adder circuit. Give the truth table and explain the operation. **(6.5)**
(b) What is binary multiplier? Discuss the multiplier using shift method. **(6)**

Q5 (a) Explain the working of BCD to seven segment decoder with diagram. **(6)**
(b) What is an encoder? Discuss the design of octal to binary encoder. **(6.5)**

UNIT-III

Q6 Discuss and explain the working of master slave JK Flip flop. What are its advantages? **(12.5)**

Q7 What is shift register? Give its classification and explain the working of each type diagram. **(12.5)**

UNIT-IV

Q8 What is modulo counter? Design a MOD-6 counter by giving all design steps. **(12.5)**

Q9 Explain the following: (a) RAM (b) PLA **(12.5)**

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END TERM EXAMINATION

SECOND SEMESTER [BCA] MAY JUNE 2017

Paper Code: BCA-106 **Subject: Digital Electronics (Batch 2011 onwards)**

Time: 3 Hours **Maximum Marks: 75**

Note: Attempt any five questions including Q.no.1 which is compulsory. Select one question from each unit.

Q1 Attempt any five from the following:- (5x5=25)

(a) Design full subtractor circuit using NAND gate only.
(b) Explain how transistor as a switch works? Give its use in logic circuits.
(c) Define fan-in, fan-out, propagation delay, noise margin and voltage parameters.
(d) Explain decoder and demultiplexer. Give their applications.
(e) State the De Morgan's theorem and prove them with an example.
(f) Define synchronous and asynchronous counters with their merit and demerits.

UNIT-I

Q2 Simply the expressions:-
(a) $AB + \bar{A}C + A\bar{B}C(AB + C)$ (3)
(b) Explain the operation and advantages of CMOS. (6.5)
(c) Prove $A + \bar{A}B = A + B$ (3)

Q3 (a) Design a combinational circuit whose input is three bit number and whose output is equal to square of input and implement it using basic gates. (6.5)
(b) Explain briefly the BCD to seven segment decoder. (6)

UNIT-II

Q4 (a) Design a full adder circuit using Multiplexer. (6.5)
(b) Implement the Ex-OR gate equation with NAND gates only. (6)

Q5 (a) Draw the logic diagram of parity checker and generator/checker. Explain its operation with the help of truth table. (6.5)
(b) Design a binary multiplier for following: A=1011, B=111 (6)

UNIT-III

Q6 (a) Define edge triggering in flip-flops. Explain Master slave JK flip-flop that solves the problem of Race-around condition, with diagram. (7)
(b) Design JK flip-flop using SR flip-flop. (5.5)

Q7 (a) Explain the bidirectional shift register with diagram, truth table and clock pulse. Give their applications. (7.5)
(b) Differentiate Static RAM and Dynamic RAM. (5)

UNIT-IV

Q8 (a) Design Modulo 7 counters with truth table and logic diagram. (7.5)
(b) Give the application of PLA and PLD. (5)

Q9 (a) Design a combinational circuit with PLA, having three inputs, four product terms and two outputs: (7.5)
F1(A,B,C)=Σ(3,5,6,7), F2(A,B,C)=Σ(0,2,4,7)
(b) Explain Johnson's counter with truth table and clock pulses. (5)

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END TERM EXAMINATION

SECOND SEMESTER [BCA] MAY-JUNE 2018

Paper Code: BCA106 ***Subject: Digital Electronics***

Time : 3 Hours ***Maximum Marks :75***

Note: Attempt any five questions including Q.no.1 which is compulsory. Select one question from each unit.

Q.1 Attempt all the questions:- **(5x5=25)**

(a) Why are NAND and NOR gates known as universal gates? Implement half adder circuit using NAND gates only.

(b) Define the terms for digital circuits:
(i) Speed of operations, (ii) Figure of Merit (iii) Noise margin.

(c) What is De-multiplexer? Explain the difference between MUX and DEMUX.

(d) What is the major disadvantage of SR flip-flop? How is this addressed in JK Fip-Flop?

(e) Explain ripple counter. What's the difference between ripple counter and synchronous counter?

Unit-I

Q.2 (a) Explain deMorgan's theorem. Prove the following using De Morgan's theorem: 8.5

(i) $AB + \overline{CD} = \overline{AB}.\overline{CD}$ and (ii) $(A+B).(C+D) = \overline{(A+B)} + \overline{(C+D)}$

(b) Implement EX-OR and EX-NOR gate using only NOR gates 4

Q.3 (a)Explain the term "logic family". Compare RTL and TTL logic. 3

(b)Simplify the following expression using K-map: 5

$Y=m_0+m_1+m_3+m_7+m_8+m_9+m_{11}+m_{15}$

(c) Prove the relationship:

(i) $\overline{A}.B.C + A.\overline{B}.C + A.B.\overline{C} + A.B.C = A.B + B.C + CA$ 3

(ii) $A.\overline{B} + A.B + B.C = A + B.C$ 1.5

UNIT-II

Q.4 (a) Explain even parity and odd parity. Design a circuit for even parity generator for 3-bit message. 5.5

(b) Show block diagram of a 3 bit parallel binary adder. 3

(c) Explain the binary multiplication method using the example (1010x1011) 4

Q.5 (a) Implement the expression using a multiplexer 6.5

$f(A,B,C\,D) = \sum m(0,2,3,6,8,9,12,14)$

(b) Design a 3:8 decoder using basic logic gates. 6

Unit III

Q.6 (a)Design a S-R latch using 2-input NOR gates 3

(b) Explain (a) J-K Flip-Flop can be converted to T Flip-Flop, (b) race around condition. 7.5

(c) Explain master-slave flip-flop 2

Q.7 (a) Justify the statement: "J-K Flip-Flop is a universal Flip-Flop. 5.5

(b)Explain the advantage of SIPO over SISO. Discuss their applications. 4

(c) What is Bi-directional Flip-Flop? 3

P.T.O.

P 1/2

Unit-IV

Q.8 (a)How ripple counter works? 2.5

(b)Show state diagram of 3 bit up/down counter. Design 3 bit up/down counter using T flip-flop. 7.5

(c) Define ring counter 2

Q.9 Write short notes on any two of the following: (6.25x2=12.5)

(i) RAM & ROM
(ii) PLA
(iii) Modulo counters

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END TERM EXAMINATION

SECOND SEMESTER [BCA] MAY-JUNE 2019

Paper Code: BCA-106 *Subject: Digital Electronics*

Time: 3 Hours *Maximum Marks: 75*

Note: Attempt any five questions including Q.no.1 which is compulsory. Select one questions from each unit. Assume missing data if any.

Q1 Attempt **any five** questions:

(a) Explain Parity Generation and checking process with example. **(4)**

(b) Explain Excess-3, BCD and gray codes. Convert binary 1101 to equivalent gray code and also convert Gray code 0111 to equivalent Binary code. **(4)**

(c) Perform the following conversions: **(3)**

(i) $(A3.1E)_{16} = (\quad)_{10}$

(ii) $(532.03)_8 = (\quad)_{16}$

(d) Define fan-in, fan-out, propagation delay, noise margin and voltage parameters. **(3)**

(e) What is a D flip flop? Show how SR flip flop can be converted to D flip flop? **(3)**

(f) Explain the working of Serial in Serial Out shift right register. **(4)**

(g) What is binary multiplier? Discuss the multiplier using shift method. **(4)**

Unit-I

Q2 (a) Design the circuit of the Boolean Equation: **(4.5)**

$Y = (\overline{A} + \overline{B})(A + \overline{C} + \overline{D})(A + \overline{B} + C)B$ using only NOR GATES.

(b) Why NAND & NOR Gates are called Universal Gates? How an AND Gate can be implemented using only NOR Gates? **(4)**

(c) Implement Ex-OR using NAND gates only. **(4)**

Q3 (a) Simplify the following Boolean Equation using Boolean Algebra Laws: **(4)**

$Y = \overline{AC(ABD)} + \overline{A}B\overline{C}D + \overline{A}B\overline{C}$

(b) Simplify the expression $\mathbf{F = \Sigma_m (0,2,3,6,7) + \Sigma_d (8,10,11,15)}$ using the K-Map method. **(4)**

(c) Express the function **Y = A + BC** in both: **(4.5)**

(i) Canonical SOP form

(ii) Canonical POS form

Unit-II

Q4 (a) Design a Full Adder Circuit using two Half Adders. **(4)**

(b) Design a 1:8 DMUX Circuit. How a 16:1 MUX can be designed using two 8:1 MUX and one OR Gate? **(4)**

(c) What is an encoder? Discuss the design of 8:3 (octal to binary) encoder. **(4.5)**

Q5 (a) What are Multiplexers & DeMultiplexers? Implement the following function using Multiplexer. **(6.5)**

$\mathbf{F(A,B,C,D) = \Sigma_m (0,1,2,3,4,6,8,9,13,14)}$

(b) Design a 4-bit Parallel Adder/Subtractor with controlled inverter and explain its working. **(6)**

P.T.O.

Unit-III

Q6 (a) Differentiate between Combinational and Sequential circuit. Design a S-R latch using 2 input NOR gates. **(6)**

(b) What is Race-Around Condition and how it can be eliminated in Master-Slave JK Flip Flop? **(6.5)**

Q7 (a) What are Shift Registers? The content of a 4-bit shift register is initially 1101. The register is shifted 4 times to the right with the serial input being 101101. What will be the final content of the register after all the 4 shifts are over? **(6)**

(b) Explain in detail the construction and working of Universal/Bi-Directional shift register. **(6.5)**

Unit-IV

Q8 (a) What is MOD 6 counter? Draw its state diagram and circuit. **(6)**

(b) Draw and Explain the working of ripple counter. **(6.5)**

Q9 (a) Differentiate between RAM and ROM. **(4)**

(b) Explain Johnson counter with truth table and clock pulses. **(4)**

(c) Draw and explain Asynchronous 3 bit up/down counter. **(4.5)**

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END TERM EXAMINATION

THIRD SEMESTER [BCA] JANUARY-FEBRUARY 2023

Paper Code: BCA-203 ***Subject: COMPUTER ORGANIZATION AND ARCHITECTURE***

Time: 3 Hours ***Maximum Marks: 75***

Note: Attempt five questions in all including Q.No.1 which is compulsory. Select one question from each unit

Q1. Attempt the following **(any five)** **[5x5=25]**

(a) Why are NAND and NOR gates known as Universal Gates? Realize Ex-OR function using only NAND gates.

(b) Differentiate De-Multiplexer and decoder.

(c) What is instruction cycle? Draw a flowchart for instruction cycle of a basic computer?

(d) What is virtual memory and how does it works?

(e) Explain the advantage of SIPO over SISO. Discuss their applications.

(f) Design 4-bit Adder-Subtractor.

UNIT-I

Q2. (a) Draw K-Map and simplify the following expression:

$$f(P, Q, R, S) = \Sigma m(0, 1, 4, 5, 7, 8, 9, 12, 13, 15)$$ **[6.5]**

(b) Design a full adder using two half adder and OR gate. **[6]**

Q3. (a) Reduce the following Boolean expression using Boolean laws.

Y=AB+A'B+AB'+(AB)' and also design using basic logic gates. **[6.5]**

(b) Design a 3:8 decoder using basic logic gates. **[6]**

UNIT-II

Q4. (a) What is shortcoming in J-K flip flop? Explain how its shortcoming is removed. Describe its operating principle. **[6.5]**

(b) Design 3-bit synchronous counter and draw output waveform. **[6]**

Q5. (a) Describe the operation of 4- bit bidirectional shift register with the help of block diagram. **[6.5]**

(b) Realize D type flip-flop using J-K flip flop. **[6]**

UNIT-III

Q6. (a) Explain instruction formats and its types using the following expression: X=(A+B)-(C+D). **[6.5]**

(b) What is register transfer language? Explain with the help of example. **[6]**

P.T.O.

BCA-203

Q7. (a) Explain the different types of addressing modes in basic computer. **[6.5]**

(b) What is meant by micro-operation? Explain the term selective set, selective compliment, selective clear micro operation? **[6]**

UNIT-IV

Q8. (a) What is asynchronous data transfer? Explain different methods of asynchronous data transfer. **[6.5]**

(b) What is DMA? Draw and explain the DMA controller in details. **[6]**

Q9. Write short notes on the following:- **[12.5]**
1. Cache Memory 2. Auxiliary Memory 3. Associative Memory 4. EPROM 5. RAM

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